NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
96-01-09	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Electronic Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	67268	5962-R032-96
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-85131**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
Microcircuit, Linear, CMOS, Multiplexer/Demultiplexer, Monolithic Silicon	a. CURRENT C	b. NEW D	5962-85131ECP-1

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "D".
Revisions description column; add "Changes in accordance with NOR 5962-R032-96".
Revisions date column; add "96-01-09".
Revision level block; change from "C" to "D".
Rev status of sheets; for sheet 1, change from "C" to "D". For sheets 24, 26, 28, 36, 37, 38, 49, 51, and 53, change from "C" to "D".

Sheets 24, 26, and 28: Table I, Break-before-make time delay, tD, and Enable to I/O, tON(EN) and tOFF(EN), Chage test condition RL from "RL = 200 Ω to "RL = 1000 Ω.
Revision level block; change "B" to "D".

Sheets 36, 37, 38, 49, 51, and 53: Figures 3 and 4, Change load resistor value from "200 Ω" to "1000 Ω".
Revision level block; change "B" to "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DESC-ELDS	Michael A. Frye

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Microelectronics Branch	Michael A. Frye	96-01-09

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED (YYMMDD)
DESC-ELDS	Sandra Rooney	96-01-09

NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD) 95-01-25

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME *(First, Middle Initial, Last)*

b. ADDRESS *(Street, City, State, Zip Code)*
Defense Electronic Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5270

5. CAGE CODE 67268

7. CAGE CODE 67268

6. NOR NO. 5962-R061-95

8. DOCUMENT NO. **5962-85131**

9. TITLE OF DOCUMENT
Microcircuit, Linear, CMOS, Multiplexer/Demultiplexer, Monolithic Silicon

10. REVISION LETTER

a. CURRENT B

b. NEW C

11. ECP NO.
No ECP necessary

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C".
Revisions description column; add "Changes in accordance with NOR 5962-R061-95".
Revisions date column; add "95-01-25".
Revision level block; add "C".
Rev status of sheets; for sheet 1, and 30, add "C".

Sheet 30: Figure 1, Terminal connections; For case outline 2, add device type 06.
Revision level block; add "C".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT
DESC-ELDS

c. TYPED NAME *(First, Middle Initial, Last)*
Michael A. Frye

d. TITLE
Chief, Microelectronics Branch

e. SIGNATURE
Michael A. Frye

f. DATE SIGNED *(YYMMDD)* 95-01-25

15a. ACTIVITY ACCOMPLISHING REVISION
DESC-ELDS

b. REVISION COMPLETED *(Signature)*
Sandra Rooney

c. DATE SIGNED *(YYMMDD)* 95-01-25

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outlines, terminal connections and thermal resistance values for case outlines 2 and 3. For device types 01, 02, and 03, add subgroup 3 to I_{IH} and I_{IL} test, add R_{DS1} test, add V_{ISO} test, delete V_{CT} test, change R_L and C_L test conditions for $t_{ON(A)}$ and $t_{OFF(A)}$ tests, change C_L test condition for $t_{ON(EN)}$ and $t_{OFF(EN)}$ tests, change value of I_D for R_{DS1} test, change value of I_D and V_S for R_{DS2} test, add test condition circuits. Editorial changes throughout.	88-08-26	D. A. DiCenzo
B	Add device types 07, 08, and 09. Table I changes. Editorial changes throughout.	93-06-28	M. A. Frye

REV	B																		
SHEET	55																		
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Marcia B. Kelleher

CHECKED BY
Ray Monnin

APPROVED BY
D. A.DiCenzo

DRAWING APPROVAL DATE
86-06-30

REVISION LEVEL B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, CMOS, MULTIPLEXER/DEMULTIPLEXER, MONOLITHIC SILICON

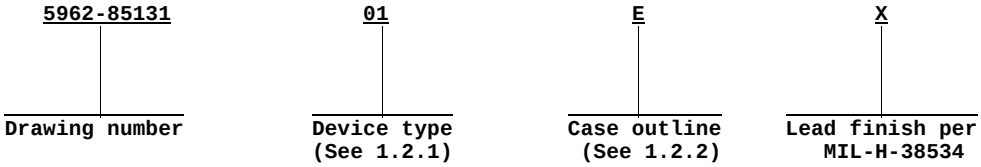
SIZE	CAGE CODE	
A	67268	5962-85131

SHEET 1 OF 55

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	546	Single 16-channel MUX/DEMUX with overvoltage protection
02	547	Differential 8-channel MUX/DEMUX with overvoltage protection
03	549	Differential 4-channel MUX/DEMUX with overvoltage protection
04	IH5116	Single 16-channel MUX/DEMUX with overvoltage protection
05	IH5216	Differential 8-channel MUX/DEMUX with overvoltage protection
06	IH5208	Differential 4-channel MUX/DEMUX with overvoltage protection
07	506	Single 16-channel MUX/DEMUX
08	507	Differential 8-channel MUX/DEMUX
09	509	Differential 4-channel MUX/DEMUX

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
X	GDIP1-T28 or CDIP-T28	28	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage between +V and -V	+44 V
Supply voltage between +V and ground:	
Device types 01-03, 07-09	+22 V
Device types 04-06	+20 V
Supply voltage between -V and ground:	
Device types 01-03, 07-09	-25 V
Device types 04-06	-20 V
Digital input voltage range (V_A, V_{EN}):	
Device types 01-03, 07-09	[(-V) -4 V) to ((+V) +4 V] or 20 mA whichever comes first
Device types 04-06	-V to +V or 20 mA whichever comes first
Analog input voltage range (V_S):	
Device types 01-03,	[(-V) -20 V) to ((+V) +20 V]
Device types 04-06	[(-V) -25 V) to (+V) +25 V]
Device types 07-09	[(-V) -2 V) to (+V) +2 V]
Continuous current, source or drain	20 mA
Peak current, source or drain, pulsed, 1 ms, 10 percent duty cycle max	40 mA
Storage temperature range	-65°C to +150°C

Maximum power dissipation (P_D):	
Case E	1.25 W
Case X	2 W
Case 2	1.32 W
Case 3	1.23 W
Derating factor:	
Case E	12.5 mW/°C above T_A = +75°C
Case X	20 mW/°C above T_A = +75°C
Case 2	13.2 mW/°C above T_A = +75°C
Case 3	12.3 mW/°C above T_A = +75°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases E, X, 2, and 3	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case E	80°C/W
Case X	50°C/W
Case 2	76°C/W
Case 3	81°C/W
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage between +V and ground	+15 V
Supply voltage between -V and ground	-15 V
V_{REF}	Open
VAL(max)	0.8 V
V_{AH}(min):	
Devices types 01-03	4.0 V
Devices types 04-09	2.4 V
V_{EN}:	
Devices types 01-03	4.0 V
Devices types 04-09	2.4 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Break-before-make test circuit and waveforms. The test circuit and waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics (device type 01).

Test	Symbol	Conditions ($V- = -15$ V, $V+ = +15$ V, $V_{EN} = 4.0$ V) $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	$V_S = +10$ V, $V_{EN} = 0.8$ V All unused inputs = -10 V $V_D = -10$ V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	$V_S = -10$ V, $V_{EN} = 0.8$ V All unused inputs = +10 V $V_D = +10$ V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	$V_D = +10$ V, $V_{EN} = 0.8$ V All unused inputs = -10 V	1	-10	+10	
			2, 3	-300	+300	
	$-I_{D(OFF)}$	$V_D = -10$ V, $V_{EN} = 0.8$ V All unused inputs = +10 V	1	-10	+10	
			2, 3	-300	+300	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	$V_D = +10$ V, $V_S = +10$ V All unused inputs = -10 V	1	-10	+10	
			2, 3	-300	+300	
	$-I_{D(ON)}$	$V_D = -10$ V, $V_S = -10$ V All unused inputs = +10 V	1	-10	+10	
			2, 3	-300	+300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 01) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$ overvoltage	V_S = 33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle	1, 2, 3	-2.0	+2.0	µA
	$-I_{D(OFF)}$ overvoltage	V_S = -33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle		-2.0	+2.0	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = -100 µA	1		1.5	kΩ
			2, 3		1.8	
	$-R_{DS1}$	V_S = -10 V I_D = +100 µA	1		1.5	
			2, 3		1.8	
Difference in switch "ON" resistance between channels	ΔR_{DS1}	T_A = +25°C $\frac{(+R_{DS1}\ max) - (+R_{DS1}\ min) \times 100}{+R_{DS1}\ Ave}$	1		7	%
		T_A = +25°C $\frac{(-R_{DS1}\ max) - (-R_{DS1}\ min) \times 100}{-R_{DS1}\ Ave}$			7	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 01) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		85	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	pF
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, 2/ C_L = 15 pF, V_S = 7 V_{rms}, f = 100 kHz T_A = +25°C	7		-50	dB
Break-before-make time delay	t_D	T_A = +25°C See figure 4	9	5		ns
Propagation delay times: Address inputs to I/O channel times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 10 MΩ C_L = 14 pF	9		500	
			10, 11		1,000	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 12.5 pF	9		500	
See figures 5 and 6			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 02) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = +10 V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-200	+200	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-200	+200	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-200	+200	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-200	+200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 02) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$ overvoltage	V_S = 33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle	1, 2, 3	-2.0	+2.0	µA
	$-I_{D(OFF)}$ overvoltage	V_S = -33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle		-2.0	+2.0	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = 100 µA	1		1.5	kΩ
			2, 3		1.8	
	$-R_{DS1}$	V_S = -10 V I_D = -100 µA	1		1.5	
			2, 3		1.8	
Difference in switch "ON" resistance between channels	ΔR_{DS1}	T_A = +25°C $(+R_{DS1}$ max) - ($+R_{DS1}$ min) x 100 / $+R_{DS1}$ Ave	1		7	%
		T_A = +25°C $(-R_{DS1}$ max) - ($-R_{DS1}$ min) x 100 / $-R_{DS1}$ Ave			7	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 02) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		50	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
OFF isolation	V_{ISO}	V_{EN} = 0.8 V, f = 100 kHz, 2/ C_L = 15 pF, V_S = 7 V_{rms} R_L = 1 kΩ TA = +25°C	7		-50	dB
Break-before-make time delay See figure 4	t_D	T_A = +25°C	9	5		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 10 MΩ C_L = 14 pF	9		500	
			10, 11		1,000	
Enable to I/O See figures 5 and 6	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 12.5 pF	9		500	
			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 03) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-100	+100	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-100	+100	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-100	+100	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-100	+100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 03) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$ overvoltage	V_S = 33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle	1, 2, 3	-2.0	+2.0	µA
	$-I_{D(OFF)}$ overvoltage	V_S = -33 V, V_D = 0 V V_{EN} = 0.8 V V_S applied at ≤ 25% duty cycle		-2.0	+2.0	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 4.0 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = 100 µA	1		1.5	kΩ
			2, 3		1.8	
	$-R_{DS1}$	V_S = -10 V I_D = -100 µA	1		1.5	
			2, 3		1.8	
Difference in switch "ON" resistance between channels	ΔR_{DS1}	T_A = +25°C $(+R_{DS1}\ max) - (+R_{DS1}\ min) \times 100 / +R_{DS1}\ Ave$	1		7	%
		T_A = +25°C $(-R_{DS1}\ max) - (-R_{DS1}\ min) \times 100 / -R_{DS1}\ Ave$			7	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 03) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		25	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		15	
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, 2/ C_L = 15 pF, V_S = 7 V_{rms}, f = 100 kHz T_A = +25°C	7		-50	dB
Break-before-make time delay See figure 4	t_D	T_A = +25°C	9	5		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 10 MΩ C_L = 14 pF	9		500	
			10, 11		1,000	
Enable to I/O See figures 5 and 6	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 12.5 pF	9		500	
			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 04) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$I_{S(OFF)}$	V_S = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-1	+1	nA
			2, 3	-50	+50	
		V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-1	+1	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-2	+2	
			2,3	-300	+300	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-2	+2	
			2, 3	-300	+300	
	$-I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-2	+2	
			2, 3 2/	-300	+300	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-2	+2	
			2, 3	-300	+300	
Leakage current from an "ON" driver into the switch (drain)	$I_{D(ON)}$	V_D = 10 V, V_S = -10 V All unused inputs = -10 V	1	-2	+2	
			2, 3	-300	+300	
		V_D = -10 V, V_S = 10 V All unused inputs = 10 V	1	-2	+2	
			2, 3	-300	+300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 04) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$I_{D(OFF)}$ overvoltage	V_S = 25 V, V_D = 0 V, V_{EN} = 0.8 V	1, 3	-2.0	+2.0	µA
			2	-5	5	
		V_S = -25 V, V_D = 0 V, V_{EN} = 0.8 V	1, 3	-2.0	+2.0	
			2	-5	5	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		mA
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	mA
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		mA
Switch "ON" resistance	R_{DS1}	V_S = 10 V, I_D = 100 µA	1, 3		1.5	kΩ
			2		2.0	
		V_S = -10 V, I_D = -100 µA	1, 3		1.5	
			2		2.0	
	R_{DS2}	V+ = 10 V, V- = -10 V, V_S = +5.0 V, I_D = 100 µA	1, 3		2.2	
			2		2.4	
		V+ = 10 V, V- = -10 V, V_S = -5.0 V, I_D = -100 µA	1, 3		2.2	
			2		2.4	
Capacitance: Address	C_A	V+ = V- = 0 V, f = 1 MHz 2/, T_A = +25°C, See 4.3.1c	4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 04) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		85	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		10	pF
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Single channel isolation	V_{ISO}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Crosstalk between channels	V_{CT}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Break-before-make time delay	t_D	T_A = +25°C 2/ See figure 4	9	5		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 1 kΩ C_L = 100 pF	9		1,000	
			10, 11		1,500	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 100 pF	9		700	
See figures 5 and 6			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 05) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$I_{S(OFF)}$	V_S = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-1	+1	nA
			2	-50	+50	
		V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-1	+1	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-2	+2	
			2, 3	-150	+150	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-2	+2	
			2, 3	-150	+150	
	$-I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-2	+2	
			2, 3	-150	+150	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-2	+2	
			2, 3	-150	+150	
Leakage current from an "ON" driver into the switch (drain)	$I_{D(ON)}$	V_D = 10 V, V_S = -10 V All unused inputs = -10 V	1	-2	+2	
			2, 3	-150	+150	
		V_D = -10 V, V_S = 10 V All unused inputs = 10 V	1	-2	+2	
			2, 3	-150	+150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 05) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$I_{D(OFF)}$ overvoltage	V_S = 25 V, V_D = 0 V, V_{EN} = 0.8 V	1, 3	-2.0	+2.0	µA
			2	-5	+5	
		V_S = -25 V, V_D = 0 V, V_{EN} = 0.8 V	1, 3	-2.0	+2.0	
			2	-5	+5	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		mA
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	mA
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		mA
Switch "ON" resistance	R_{DS1}	V_S = 10 V, I_D = 100 µA	1, 3		1.5	kΩ
			2		2.0	
		V_S = -10 V, I_D = -100 µA	1, 3		1.5	
			2		2.0	
	R_{DS2} 2/	V+ = 10 V, V- = -10 V, V_S = +5.0 V, I_D = 100 µA	1, 3		2.2	
			2		2.4	
		V+ = 10 V, V- = -10 V, V_S = -5.0 V, I_D = -100 µA	1, 3		2.2	
			2		2.4	
Capacitance: Address	C_A	V+ = V- = 0 V 2/, f = 1 MHz, T_A = +25°C	4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 05) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		85	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		10	pF
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Single channel isolation	V_{ISO}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Crosstalk between channels	V_{CT}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Break-before-make time delay See figure 4	t_D	T_A = +25°C 2/ See figure 4	9	5		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 1 kΩ C_L = 100 pF	9		1,000	ns
			10, 11		1,500	ns
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 100 pF	9		700	ns
See figures 5 and 6			10, 11		1,000	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 06) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 3	-1.0	1.0	µA
	I_{IL}		2		10	
Leakage current into the source terminal of an "OFF" switch	$I_{S(OFF)}$	V_S = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-1	+1	nA
			2, 3	-50	+50	
		V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-1	+1	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-1	+1	nA
			2, 3	-100	+100	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-1	+1	
			2, 3	-100	+100	
	$-I_{D(OFF)}$	V_D = 10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-1	+1	nA
			2, 3	-100	+100	
		V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-1	+1	
			2, 3	-100	+100	
Leakage current from an "ON" driver into the switch (drain)	$I_{D(ON)}$	V_D = 10 V, V_S = -10 V All unused inputs = -10 V	1	-2	+2	nA
			2, 3	-100	+100	
		V_D = -10 V, V_S = 10 V All unused inputs = 10 V	1	-2	+2	
			2, 3	-100	+100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 06) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$I_{D(OFF)}$ overvoltage	V_S = 25 V, V_D = 0 V V_{EN} = 0.8 V	1, 3	-2.0	+2.0	µA
			2	-5	5	
		V_S = -25 V, V_D = 0 V V_{EN} = 0.8 V	1, 3	-2.0	+2.0	
			2	-5	5	
Positive supply current	I(+)	V_A = 5 V, V_{EN} = 2.4 V	1, 2, 3		2.0	mA
Negative supply current	I(-)	V_A = 5 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		mA
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.0	mA
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		mA
Switch "ON" resistance	R_{DS1}	V_S = 10 V I_D = 100 µA	1, 3		1.5	kΩ
			2		2.0	
		V_S = -10 V I_D = -100 µA	1, 3		1.5	
			2		2.0	
	R_{DS2} 2/	V+ = 10 V, V- = -10 V, V_S = +5.0 V I_D = 100 µA	1, 3		2.2	
			2		2.4	
		V+ = 10 V, V- = -10 V, V_S = -5.0 V I_D = -100 µA	1, 3		2.2	
			2		2.4	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C	4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 06) - Continued.

Test	Symbol	Conditions 3/ (V- = -15 V, V+ = +15 V, V_{EN} = 2.4 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		85	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz 2/ T_A = +25°C See 4.3.1c	4		10	pF
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Single channel isolation	V_{ISO}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Crosstalk between channels	V_{CT}	V_{GEN} = 1 V, f = 200 kHz 2/ T_A = +25°C	7		-50	dB
Break-before-make time delay See figure 4	t_D	T_A = +25°C 2/	9	5		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 1 kΩ C_L = 100 pF	9		1,000	
			10, 11		1,500	
Enable to I/O See figures 5 and 6	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 100 pF	9		700	
			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 07) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = +10 V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-300	+300	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-300	+300	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-300	+300	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-300	+300	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3		3.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		3.0	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 07) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = 1 mA	1		300	Ω
			2, 3		400	
	$-R_{DS1}$	V_S = -10 V I_D = -1 mA	1		300	
			2, 3		400	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		12	pF
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		90	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		12	
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, 2/ C_L = 15 pF, V_S = 7 V_{rms}, f = 100 kHz T_A = +25°C	7	-50		dB
Break-before-make time delay, see figure 4	t_D	R_L = 200Ω, C_L = 12.5 pF, T_A = +25°C	9	25		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 200Ω C_L = 12.5 pF	9		500	
			10, 11		1,000	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 200Ω C_L = 12.5 pF	9		500	
See figures 5 and 6			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 08) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-200	+200	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-200	+200	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-200	+200	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-200	+200	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3		3.0	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		3.0	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 08) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = 1 mA	1		300	Ω
			2, 3		400	
	$-R_{DS1}$	V_S = -10 V I_D = -1 mA	1		300	
			2, 3		400	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		12	pF
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		50	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		12	
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, 2/ C_L = 15 pF, V_S = 7 V_{rms}, f = 100 kHz T_A = +25°C	7	-50		dB
Break-before-make time delay, see figure 4	t_D	R_L = 200Ω, C_L = 12.5 pF, T_A = +25°C	9	25		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 200Ω C_L = 12.5 pF	9		500	
			10, 11		1,000	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 200Ω C_L = 12.5 pF	9		500	
See figures 5 and 6			10, 11		1,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 09) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current 1/	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3		1.0	µA
	I_{IL}				1.0	
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V V_D = -10 V	1	-10	+10	nA
			2, 3	-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V V_D = 10 V	1	-10	+10	
			2, 3	-50	+50	
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-100	+100	
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-100	+100	
Leakage current from an "ON" driver into the switch (drain)	$+I_{D(ON)}$	V_D = +10 V, V_S = +10 V All unused inputs = -10 V	1	-10	+10	
			2, 3	-100	+100	
	$-I_{D(ON)}$	V_D = -10 V, V_S = -10 V All unused inputs = +10 V	1	-10	+10	
			2, 3	-100	+100	
Positive supply current	I(+)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3		2.4	mA
Negative supply current	I(-)	V_A = 0 V, V_{EN} = 2.4 V	1, 2, 3	-1.0		
Standby positive supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3		2.4	
Standby negative supply current	$-I_{SBY}$	V_A = 0 V, V_{EN} = 0 V	1, 2, 3	-1.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 09) - Continued.

Test	Symbol	Conditions (V- = -15 V, V+ = +15 V, V_{EN} = 4.0 V) -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Switch "ON" resistance	$+R_{DS1}$	V_S = 10 V I_D = 1 mA	1		300	Ω
			2, 3		400	
	$-R_{DS1}$	V_S = -10 V I_D = -1 mA	1		300	
			2, 3		400	
Capacitance: Address	C_A	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		10	pF
Capacitance: Output switch	C_{OS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		25	pF
Capacitance: Input switch	C_{IS}	V+ = V- = 0 V f = 1 MHz T_A = +25°C See 4.3.1c	4		12	
Charge transfer error	V_{CTE}	V_S = GND 2/ V_{GEN} = 0 V to 5 V T_A = +25°C	7		10	mV
Off isolation	V_{ISO}	V_{EN} = 0.8 V, R_L = 1 kΩ, 2/ C_L = 15 pF, V_S = 7 V_{rms}, f = 100 kHz T_A = +25°C	7	-50		dB
Break-before-make time delay, see figure 4	t_D	R_L = 200Ω, C_L = 12.5 pF, T_A = +25°C	9	25		ns
Propagation delay times: Address inputs to I/O channels times: See figures 5 and 6	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 10 MΩ C_L = 14 pF	9		500	
			10, 11		1,000	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 200Ω C_L = 12.5 pF	9		500	
See figures 5 and 6			10, 11		1,000	

See footnotes at end on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ Input current of one input mode.
2/ Guaranteed, if not tested, to the limits as specified.
3/ Current flowing in either direction between any associated input and output terminals of the switch shall be 30 mA.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 capacitance measurements shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

Case Outline	E	X	X	X	X	2	3	3	3	3
Device Type	03,06,09	01	02	04,07	05,08	03,09	01	02	07	08
Terminal number	Terminal Symbol									
1	A0	V+	V+	V+	V+	NC	V+	V+	V+	V+
2	ENABLE	NC	OUT B	NC	OUT B	A0	NC	OUT B	NC	OUT B
3	V-	NC	NC	NC	NC	ENABLE	NC	NC	NC	NC
4	IN 1A	IN 16	IN 8B	IN 16	IN 8B	V-	IN 16	IN 8B	IN 16	IN 8B
5	IN 2A	IN 15	IN 7B	IN 15	IN 7B	IN 1A	IN 15	IN 7B	IN 15	IN 7B
6	IN 3A	IN 14	IN 6B	IN 14	IN 6B	NC	IN 14	IN 6B	IN 14	IN 6B
7	IN 4A	IN 13	IN 5B	IN 13	IN 5B	IN 2A	IN 13	IN 5B	IN 13	IN 5B
8	OUT A	IN 12	IN 4B	IN 12	IN 4B	IN 3A	IN 12	IN 4B	IN 12	IN 4B
9	OUT B	IN 11	IN 3B	IN 11	IN 3B	IN 4A	IN 11	IN 3B	IN 11	IN 3B
10	IN 4B	IN 10	IN 2B	IN 10	IN 2B	OUT A	IN 10	IN 2B	IN 10	IN 2B
11	IN 3B	IN 9	IN 1B	IN 9	IN 1B	NC	IN 9	IN 1B	IN 9	IN 1B
12	IN 2B	GND	GND	GND	GND	OUT B	GND	GND	GND	GND
13	IN 1B	V REF	V REF	NC	NC	IN 4B	V REF	V REF	NC	NC
14	V+	A3	NC	A3	NC	IN 3B	A3	NC	A3	NC
15	GND	A2	A2	A2	A2	IN 2B	A2	A2	A2	A2
16	A1	A1	A1	A1	A1	NC	A1	A1	A1	A1
17	---	A0	A0	A0	A0	IN 1B	A0	A0	A0	A0
18	---	ENABLE	ENABLE	ENABLE	ENABLE	V+	ENABLE	ENABLE	ENABLE	ENABLE
19	---	IN 1	IN 1A	IN 1	IN 1A	GND	IN 1	IN 1A	IN 1	IN 1A
20	---	IN 2	IN 2A	IN 2	IN 2A	A1	IN 2	IN 2A	IN 2	IN 2A
21	---	IN 3	IN 3A	IN 3	IN 3A	---	IN 3	IN 3A	IN 3	IN 3A
22	---	IN 4	IN 4A	IN 4	IN 4A	---	IN 4	IN 4A	IN 4	IN 4A
23	---	IN 5	IN 5A	IN 5	IN 5A	---	IN 5	IN 5A	IN 5	IN 5A
24	---	IN 6	IN 6A	IN 6	IN 6A	---	IN 6	IN 6A	IN 6	IN 6A
25	---	IN 7	IN 7A	IN 7	IN 7A	---	IN 7	IN 7A	IN 7	IN 7A
26	---	IN 8	IN 8A	IN 8	IN 8A	---	IN 8	IN 8A	IN 8	IN 8A
27	---	V-	V-	V-	V-	---	V-	V-	V-	V-
28	---	OUT	OUT A	OUT	OUT A	---	OUT	OUT A	OUT A	OUT A

FIGURE 1. Terminal connections.

Device types 01, 04, and 07

A3	A2	A1	AO	EN	CHANNEL SELECTED
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

Device types 02, 05, and 08

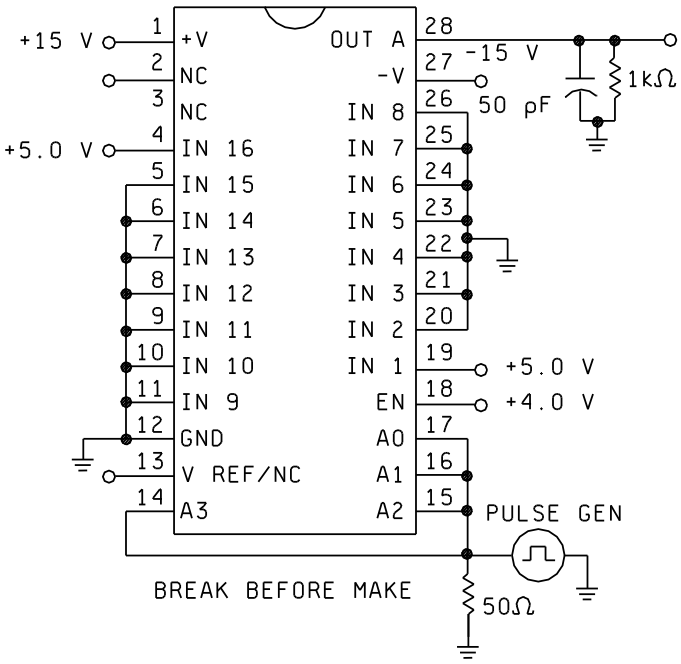
A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	L	NONE
L	L	L	H	1A,1B
L	L	H	H	2A,2B
L	H	L	H	3A,3B
L	H	H	H	4A,4B
H	L	L	H	5A,5B
H	L	H	H	6A,6B
H	H	L	H	7A,7B
H	H	H	H	8A,8B

Device types 03, 06, and 09

A1	A0	EN	CHANNEL SELECTED
X	X	L	NONE
L	L	H	1A,1B
L	H	H	2A,2B
H	L	H	3A,3B
H	H	H	4A,4B

FIGURE 3. Truth tables.

Device type 01



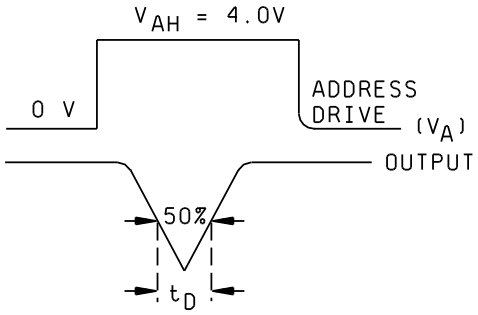
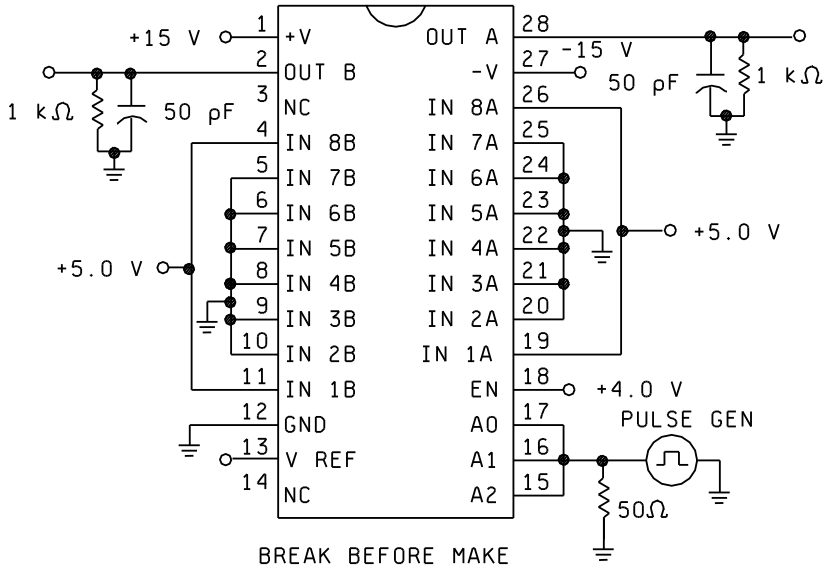


FIGURE 3. Break-before-make test circuit and waveforms.

Device type 02



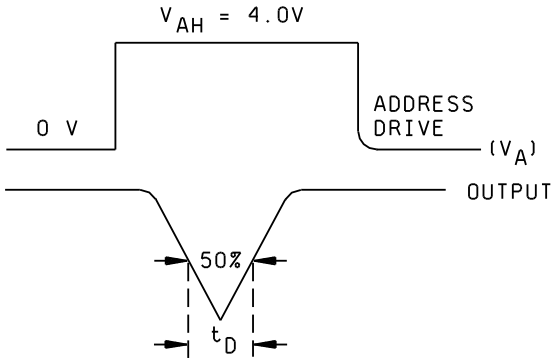
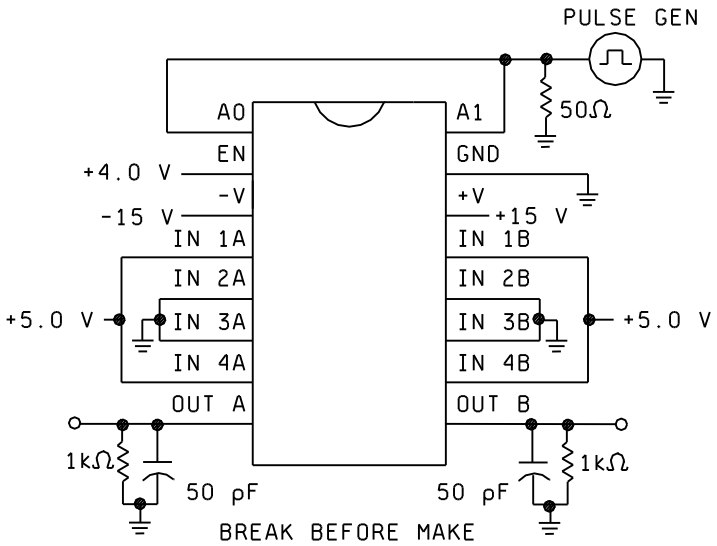


FIGURE 3. **Break-before-make test circuit and waveforms** - **Continued.**

Device type 03



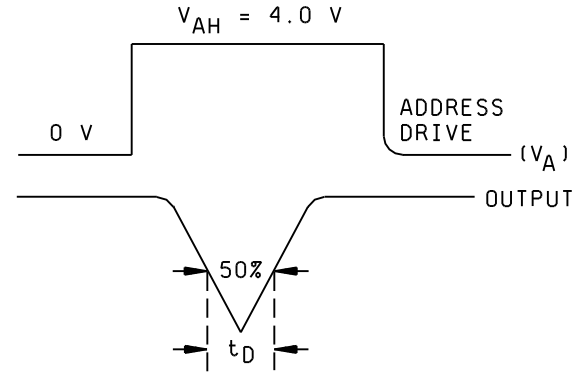
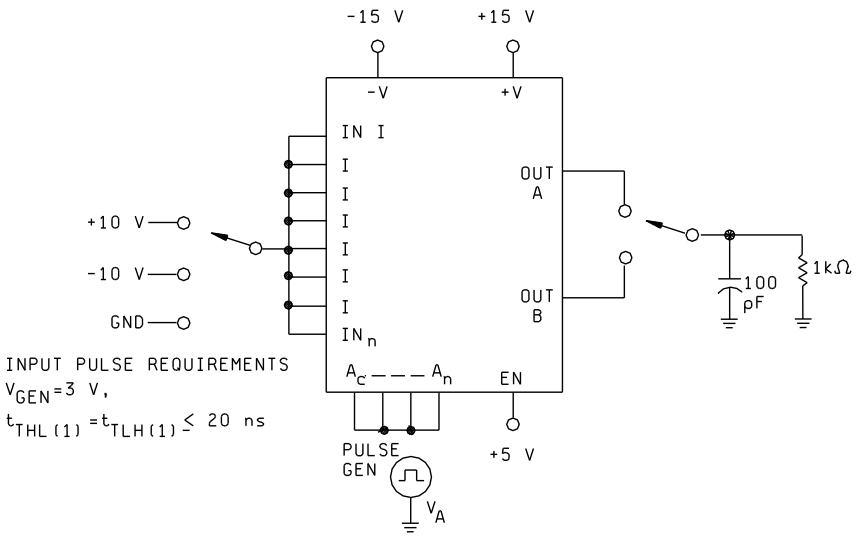


FIGURE 3. Break-before-make test circuit and waveforms - Continued.

Device types 04, 05, and 06



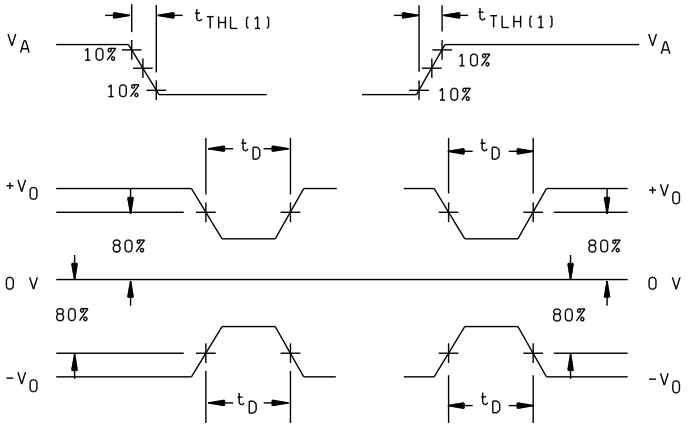
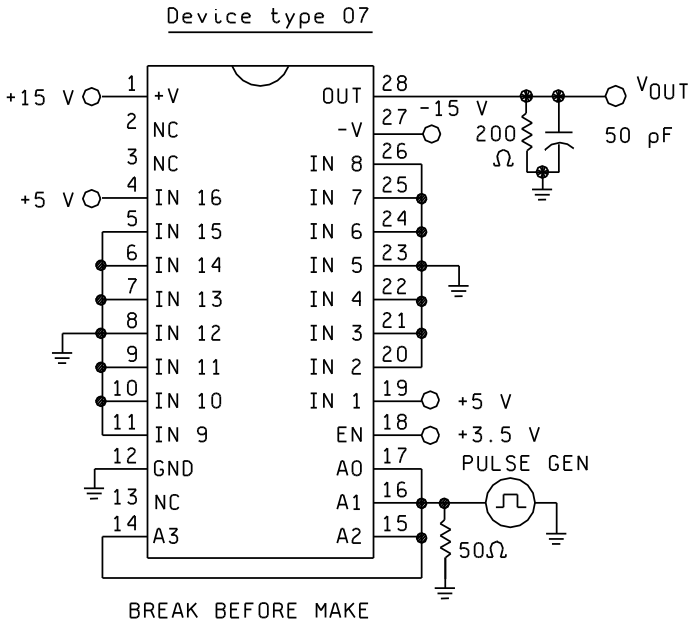


FIGURE 3. **Break-before-make test circuit and waveforms** - **Continued.**



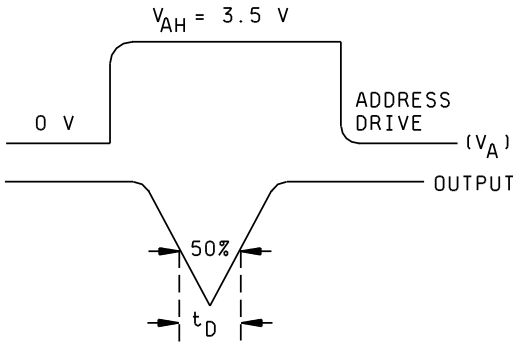


FIGURE 3. **Break-before-make test circuit and waveforms - Continued.**

Device type 08

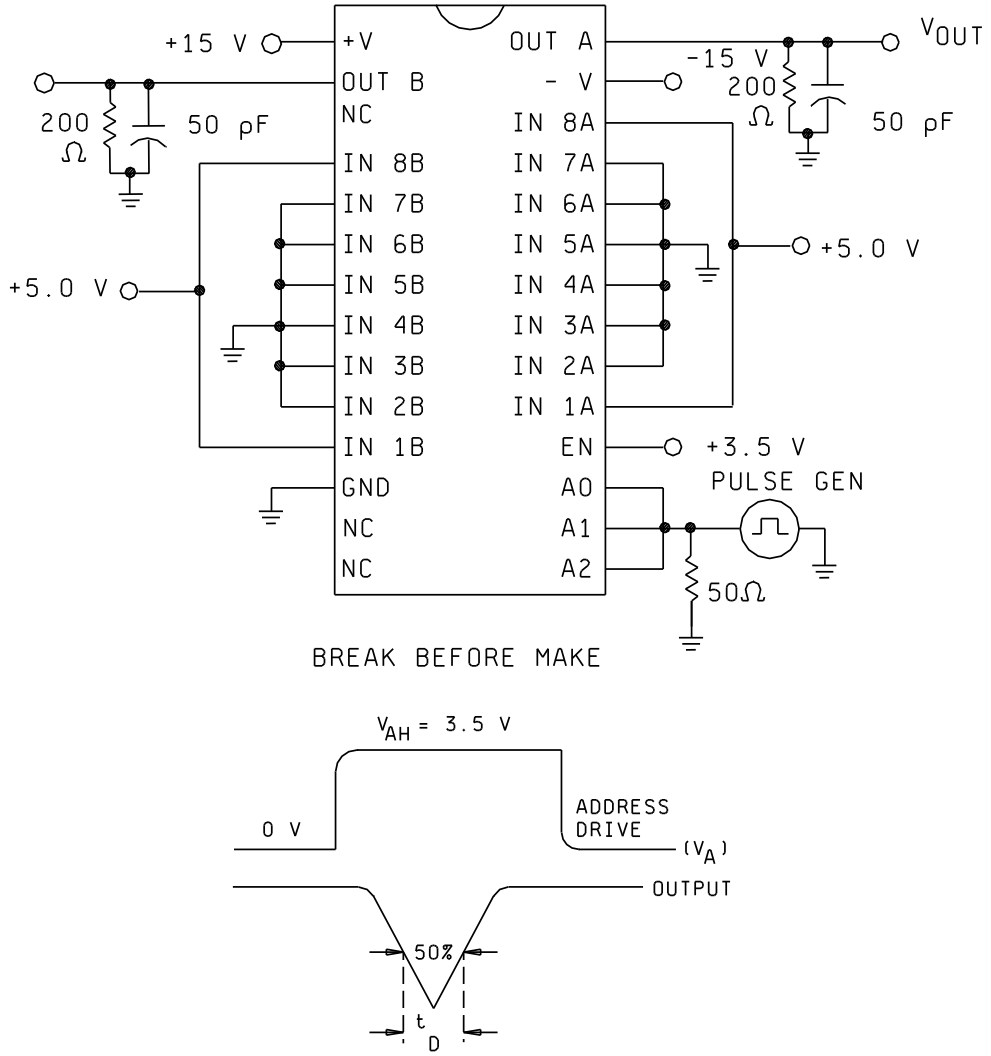
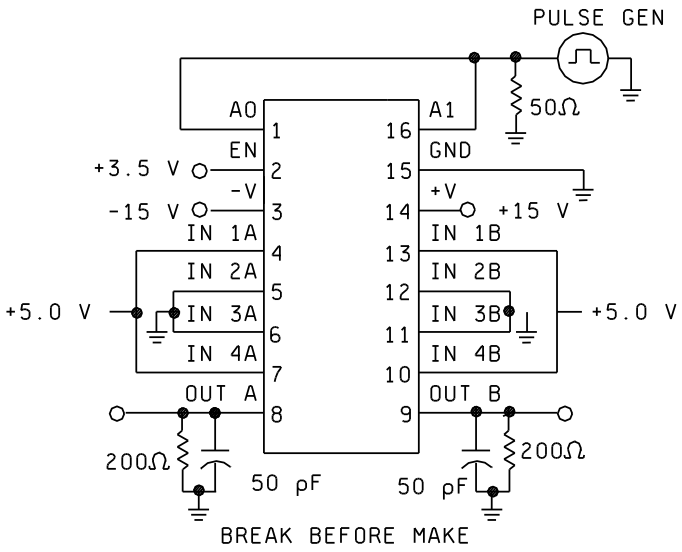


FIGURE 3. Break-before-make test circuit and waveforms - Continued.

Device type 09



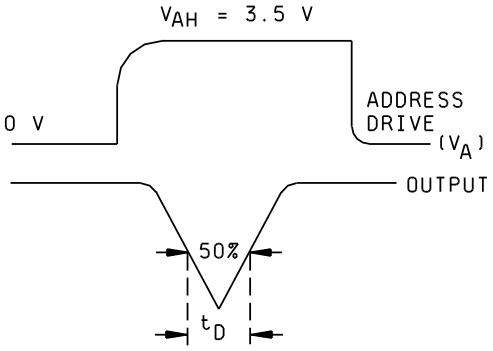
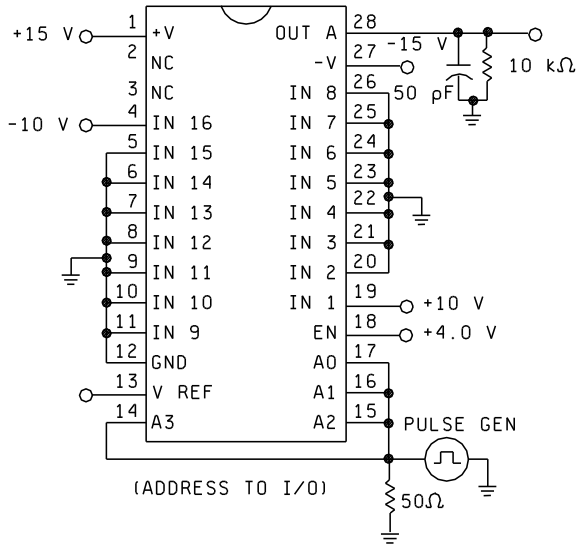


FIGURE 3. **Break-before-make test circuit and waveforms** - **Continued.**

Device type 01



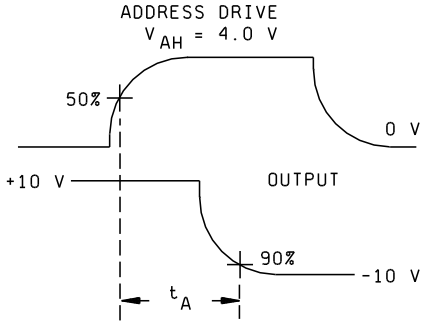
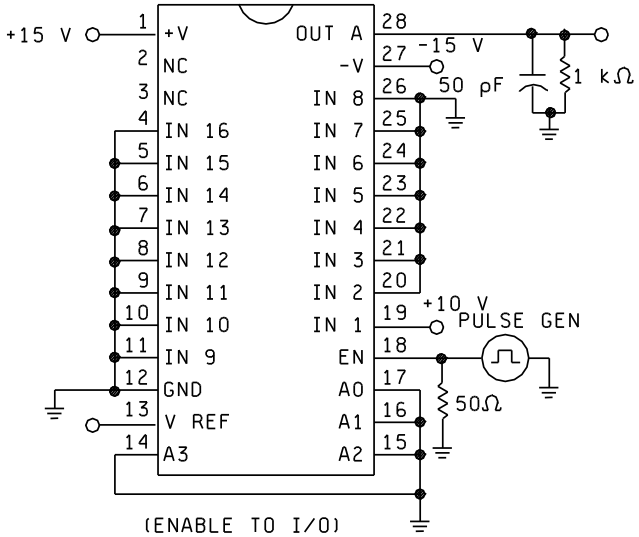


FIGURE 4. Switching times test circuits.

Device type 01



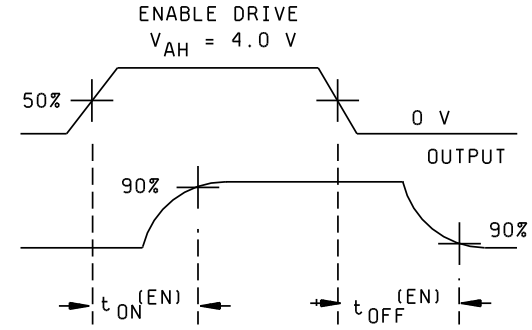
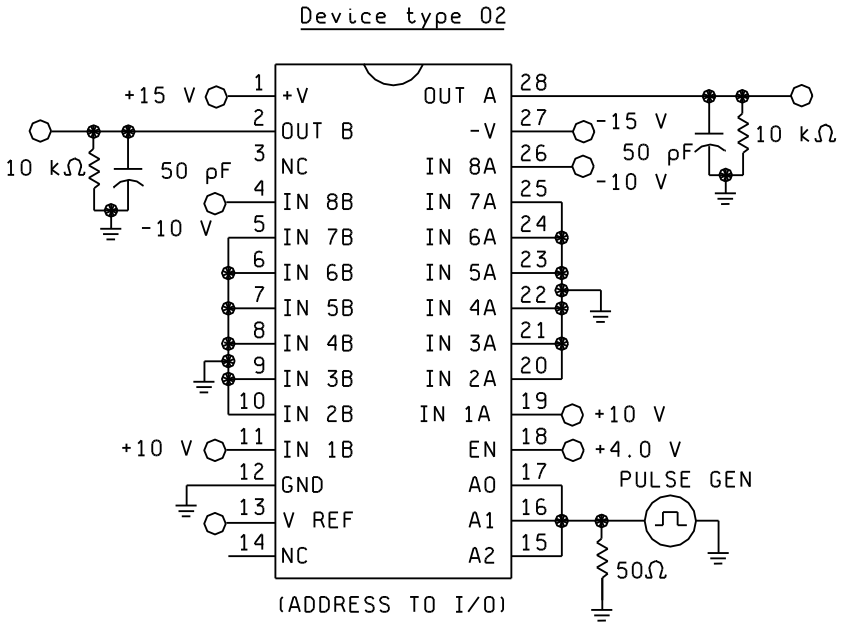


FIGURE 4. Switching times test circuits - Continued.



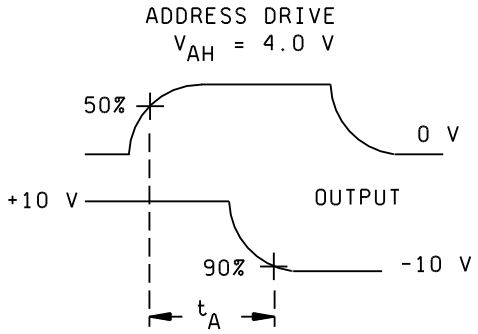
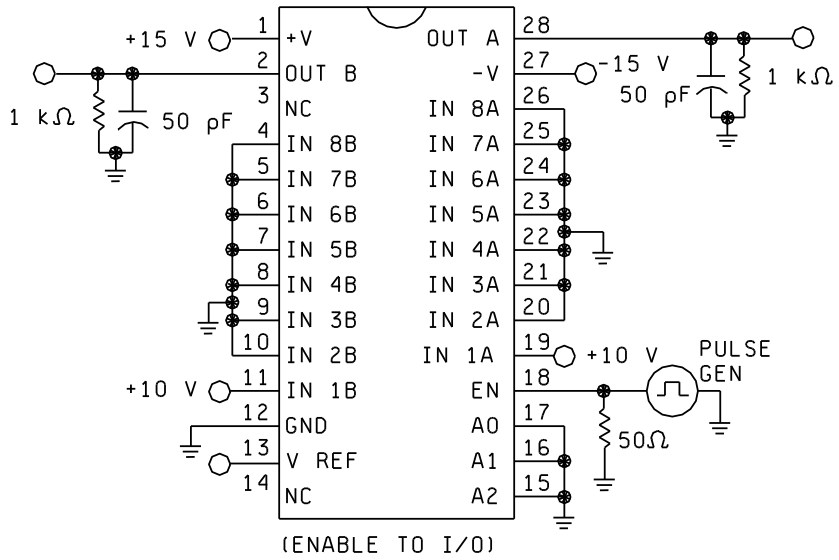


FIGURE 4. Switching times test circuits - Continued.

Device type 02



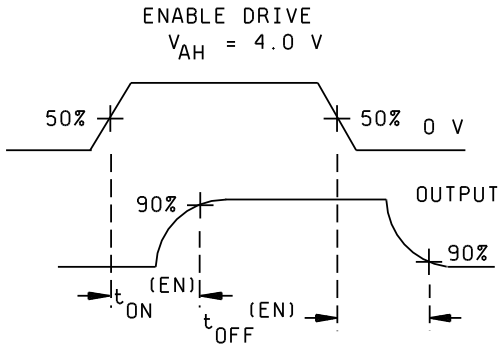
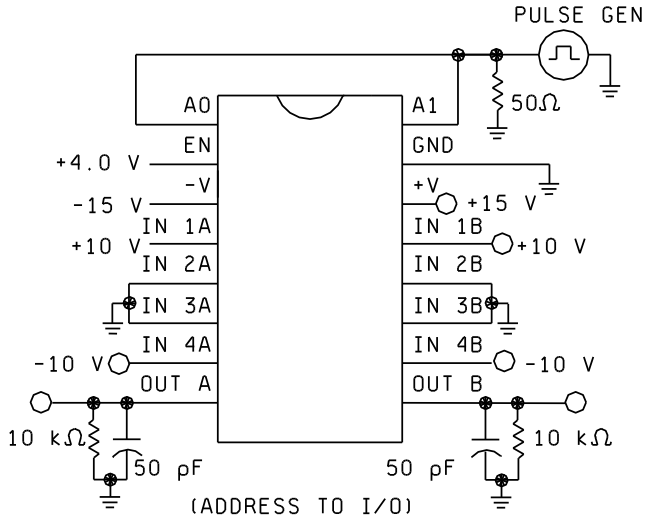


FIGURE 4. Switching times test circuits - Continued.

Device type 03



ADDRESS DRIVE

V_{AH} = 4.0 V for device type 03

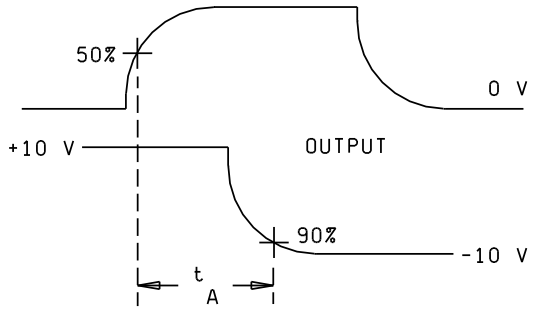
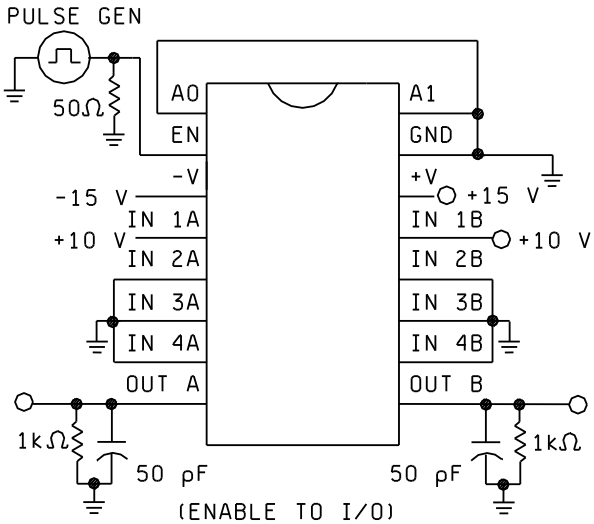


FIGURE 4. **Switching times test circuits** **- Continued.**

Device type 03



ENABLE DRIVE

V_{AH} = 4.0 V for device type 03

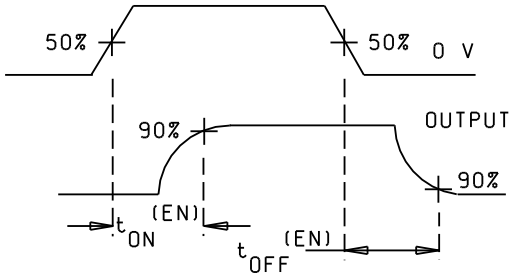
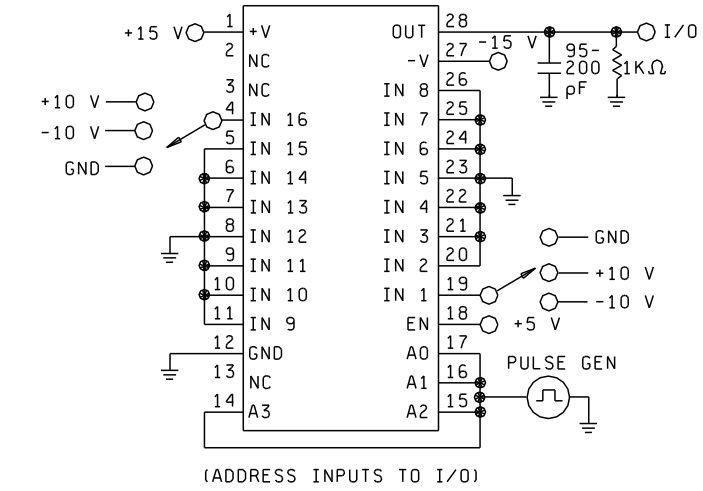


FIGURE 4. Switching times test circuits - Continued.

Device type 04



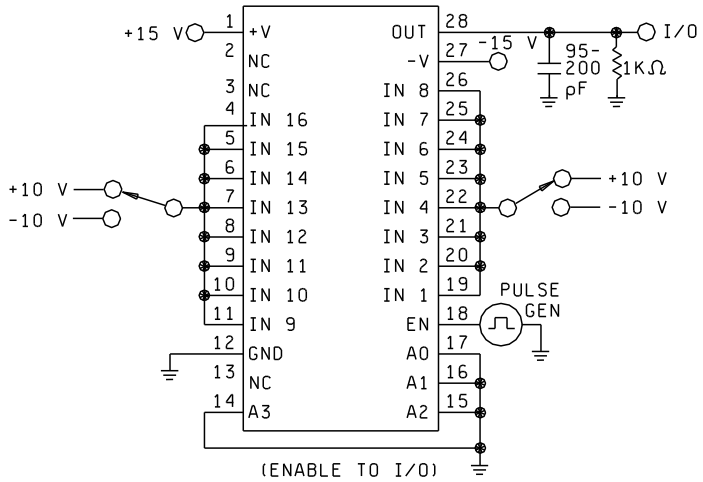
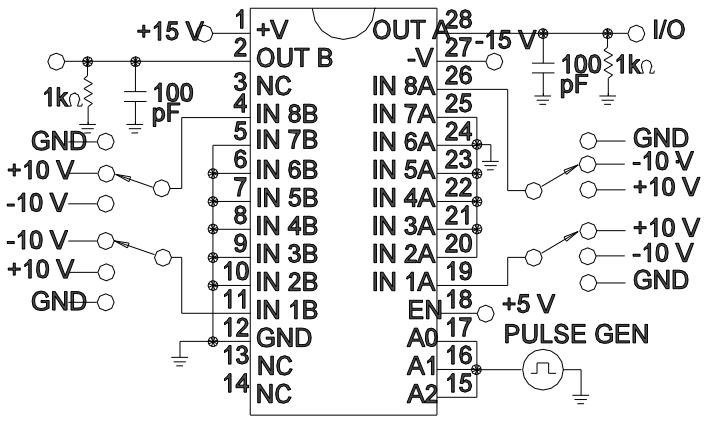
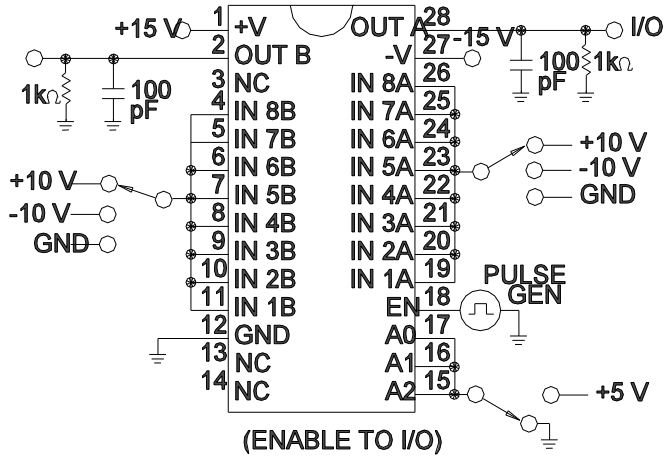


FIGURE 4. Switching times test circuits - Continued.

Device type 05



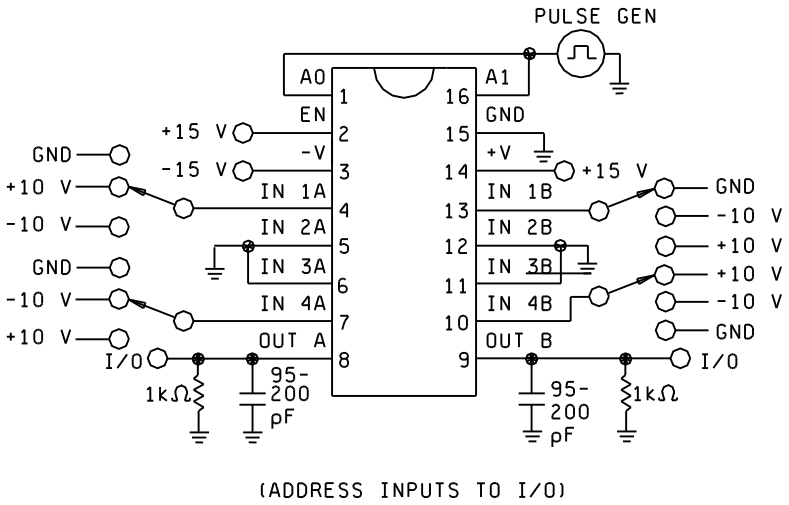
(ADDRESS INPUTS TO I/O)



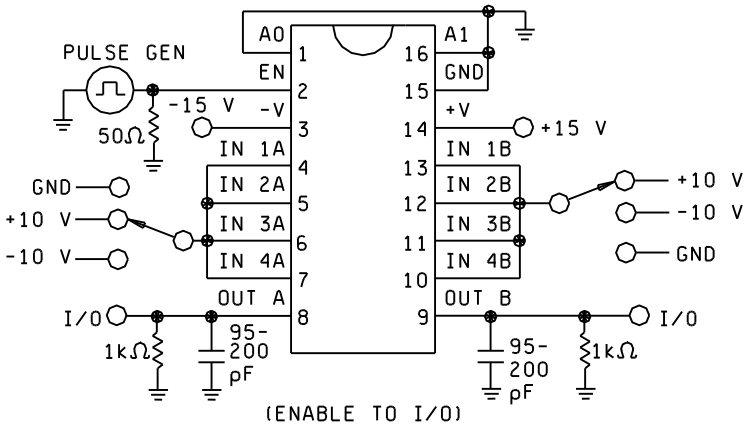
(ENABLE TO I/O)

FIGURE 4. Switching times test circuits - Continued.

Device type 06



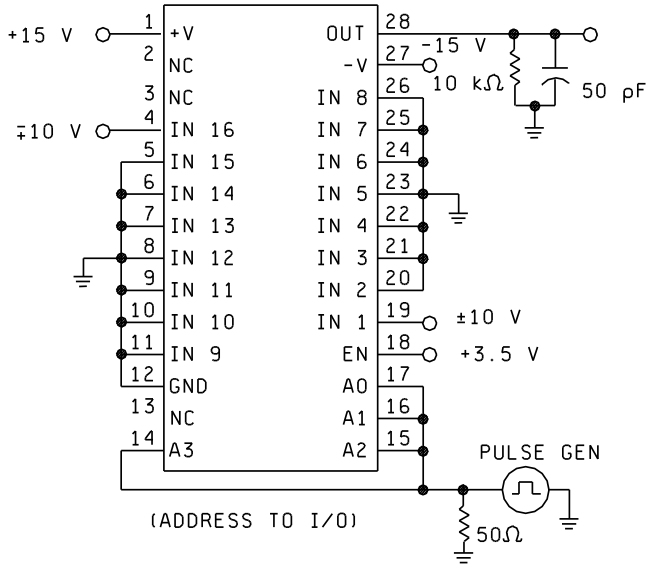
(ADDRESS INPUTS TO I/O)



(ENABLE TO I/O)

FIGURE 4. Switching times test circuits - Continued.

Device type 07



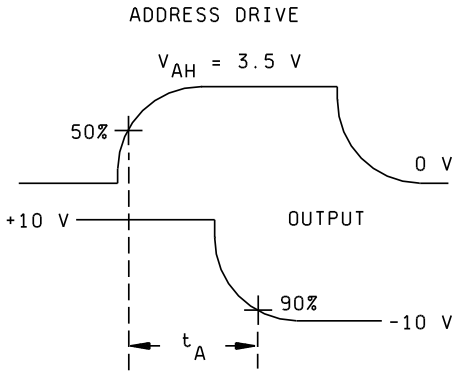
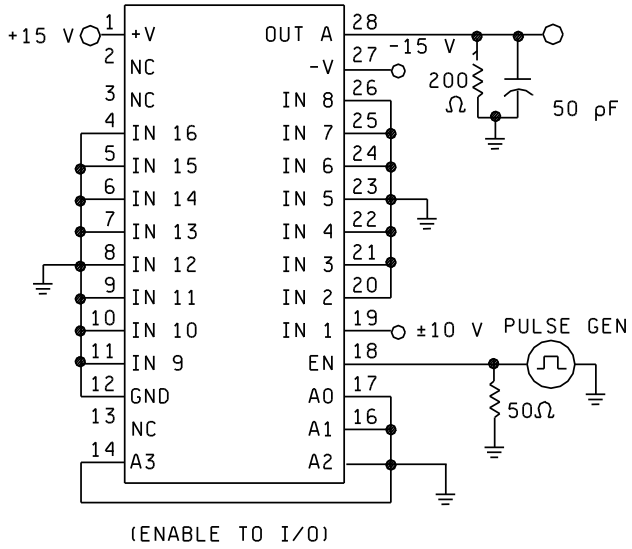


FIGURE 4. **Switching times test circuits** **- Continued.**

Device type 07



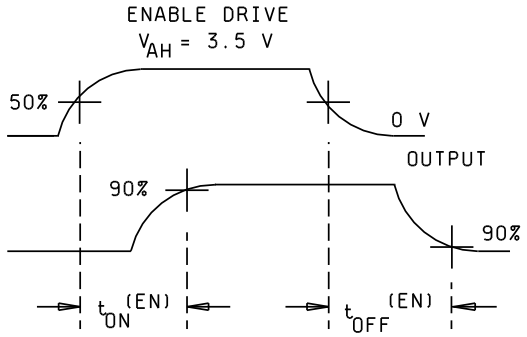
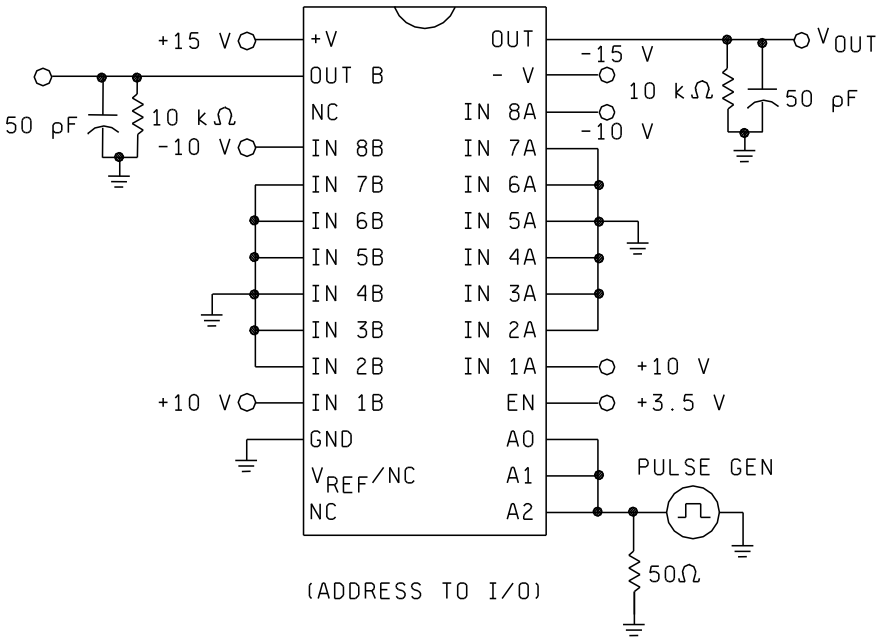


FIGURE 4. **Switching times test circuits** **- Continued.**

Device type 08



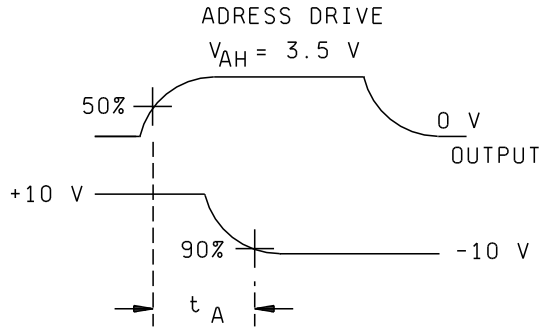
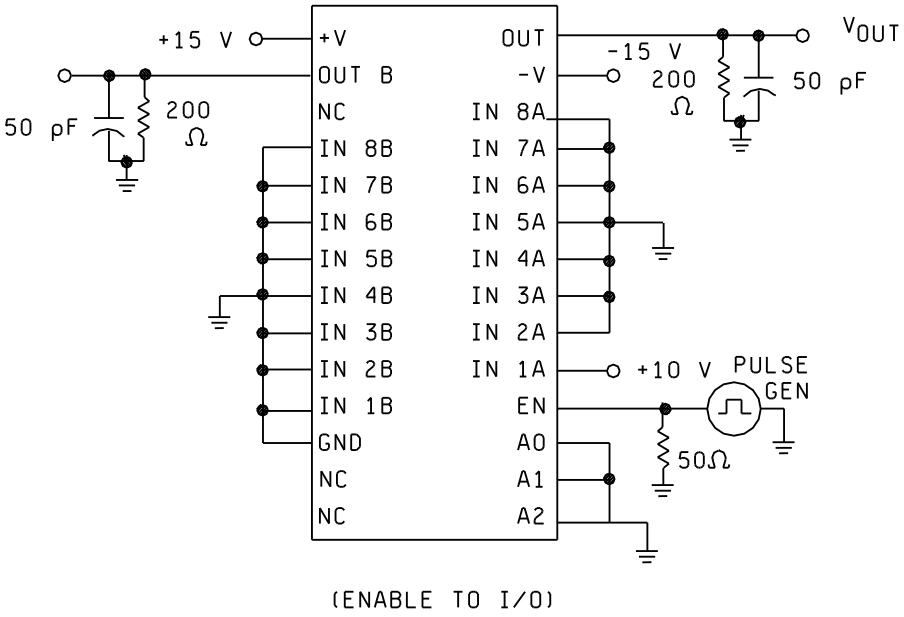


FIGURE 4. **Switching times test circuits** **- Continued.**

Device type 08



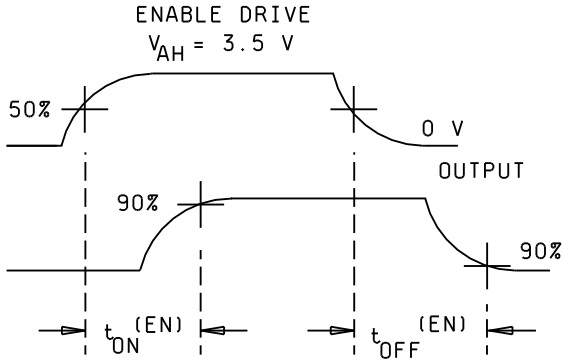
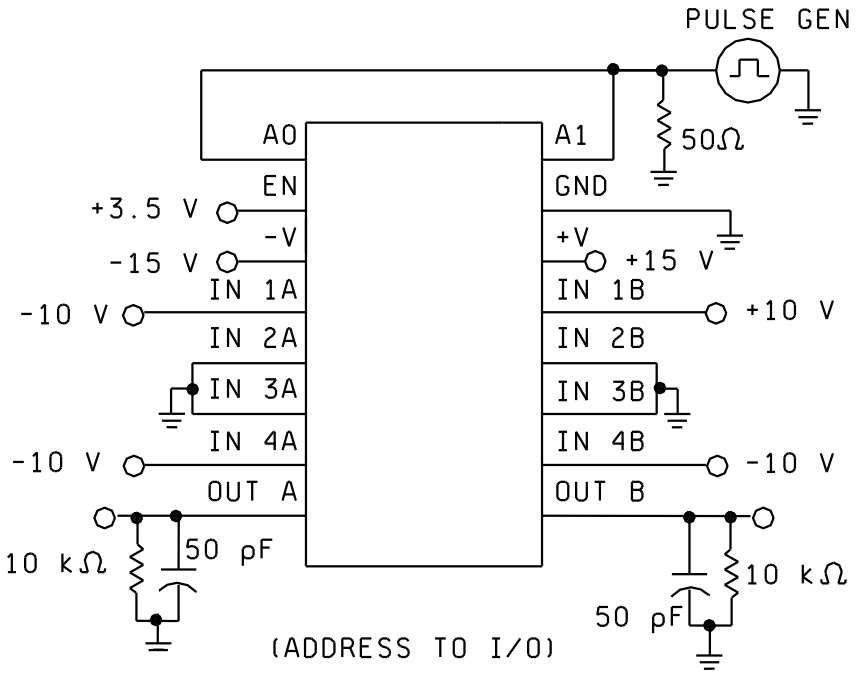


FIGURE 4. **Switching times test circuits** **- Continued.**

Device type 09



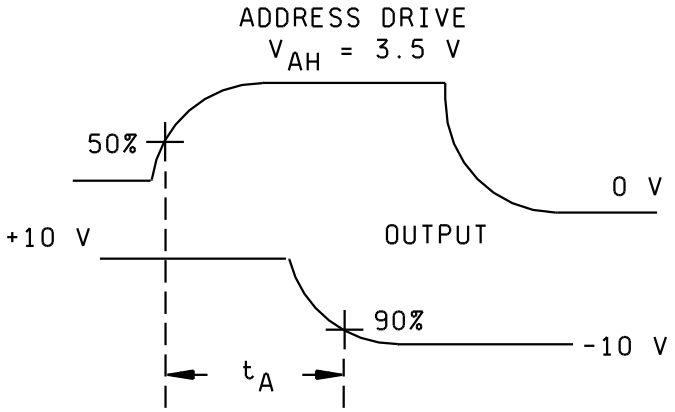
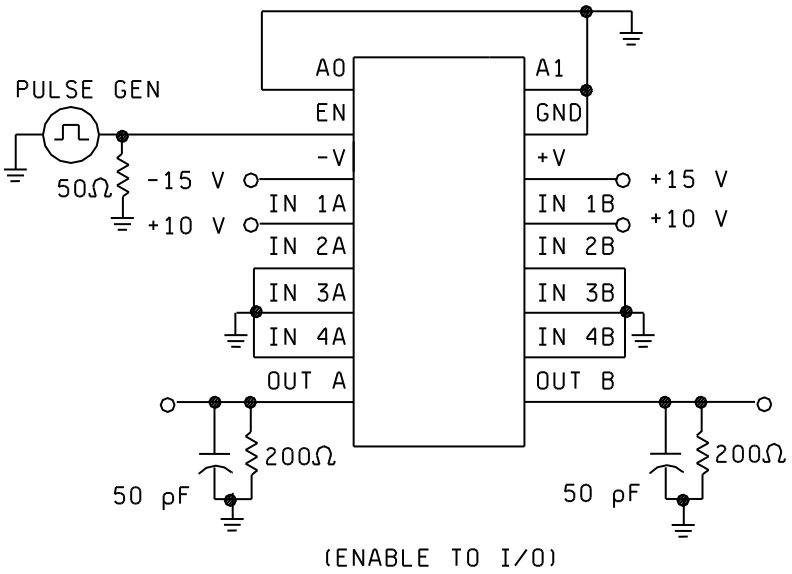


FIGURE 4. Switching times test circuits - Continued.

Device type 09



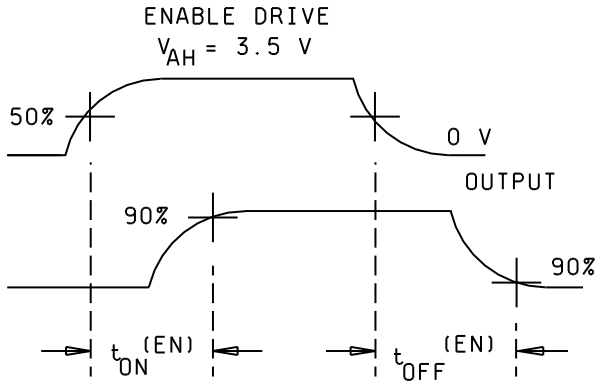
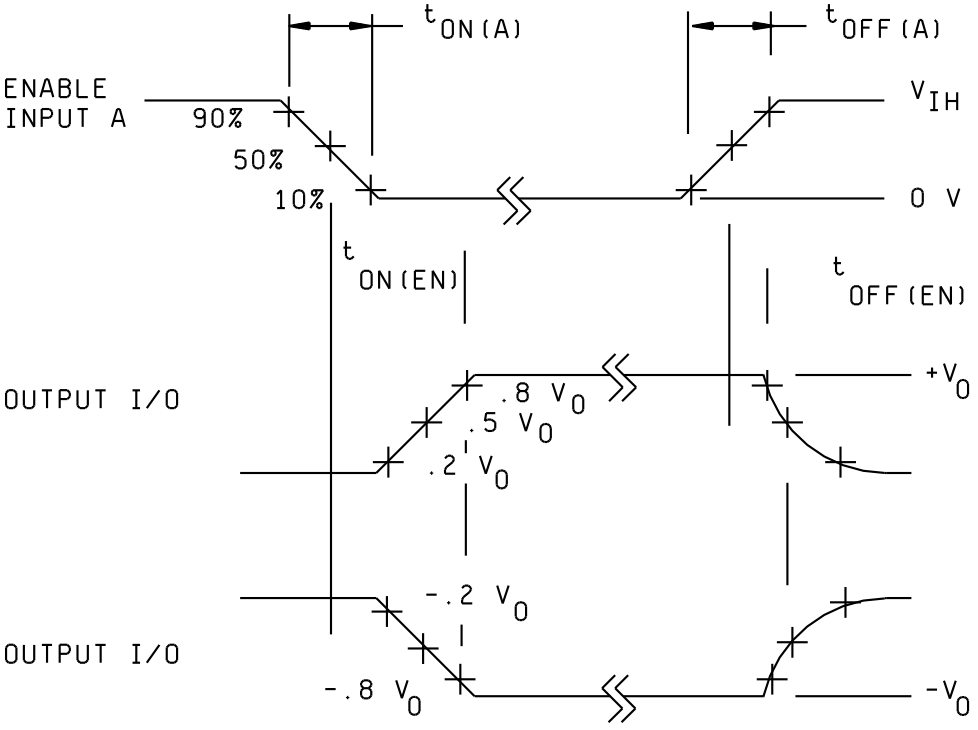


FIGURE 4. Switching times test circuits - Continued.

Device types 04, 05, and 06



INPUT PULSE REQUIREMENTS
V_{GEN} = 3 V
$t_{THL(1)} = t_{TLH(1)} \leq 20$ ns

FIGURE 4. Switching times test circuits - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-8527.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE:

Approved sources of supply for SMD 5962-85131 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of QML-38534.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification part number
5962-8513101XX 2/	34371	HI1-546/883	M38510/19002BXX
5962-85131013X	34371	HI4-546/883	---
5962-8513102XX 2/	34371	HI1-547/883	M38510/19004BXX
5962-85131023X	34371	HI4-547/883	---
5962-8513103EX 2/	34371	HI1-549/883	M38510/19006BEX
5962-85131032X	34371	HI4-549/883	---
5962-8513104XX 2/	32293	IH5116MJI	M38510/19002BXX
5962-8513105XX 2/	32293	IH5216MJI	M38510/19004BXX
5962-8513106EX 2/	32293	IH5208MJE	M38510/19006BEX
5962-8513107XX 2/	34371	HI1-506/883	M38510/19001BXX
5962-85131073X	34371	HI4-506/883	---
5962-8513108XX 2/	34371	HI1-507/883	M38510/19003BXX
5962-85131003X	34371	HI4-507/883	---
5962-8513109EX 2/	34371	HI1-509/883	M38510/19008BEX
5962-85131092X	34371	HI4-509/883	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design, use QPL M38510 product.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O Box 883 Melbourne, FL 32902-0883

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